REMARKS

Claims 1-34 are pending in the present application. Claims 1, 2, 4-9, 11-18, 20-29, and 31-34 were examined, claims 3, 10, 19, and 30 were withdrawn.

In the office action mailed June 17, 2006 (the "Office Action"), the Examiner rejected claims 1, 2, 5, 6, 8, 9, 13, 14, 17, 18, 21, 22, 24, 26, 28, 29, 32, and 33 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,477,614 to Leddige *et al.* (the "Leddige patent") in view of U.S. Patent Publication No. 2004/0216018 to Cheung (the "Cheung reference"). The Examiner further rejected claims 7, 12, 23, and 34 under 35 U.S.C. 103(a) as being unpatentable over the Leddige patent in view of the Cheung patent, and further in view of U.S. Patent No. 6,782,465 to Schmidt (the "Schmidt patent"). Claims 4, 11, 20, and 31 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Leddige and Cheung patents, and further in view of Jones, Throughput Expansion with FET Based Crossbar Switching (the "Jones reference"). Claims 15, 16, 25, and 27, have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Leddige and Cheung patents, and further in view of U.S. Patent Publication No. 2004/0243769 to Frame *et al.* (the "Frame reference"). The Examiner further indicated that the Declaration under 37 C.F.R. 1.131 (the "131 declaration") had been considered but was found ineffective to overcome the Cheung reference.

An information disclosure statement was submitted on June 26, 2006 (the "IDS"). Applicant requests the Examiner consider the reference cited in the Form PTO-1449 of the IDS and provide the attorney of record with a signed and initialed copy of the Form PTO-1449.

The Examiner argues that the 131 declaration did not sufficiently establish conception of all of the claimed limitations, identifying dependent claims as evidence of the deficiency. *See* the Office Action at page 10. The Examiner further argues that due to claiming conception of at least claims 1, 8, 13, and 24, the conception of the other pending claims is in question. *See* the Office Action at page 12. The Examiner does not address whether conception of at least claims 1, 8, 13, and 24 has been established. The figures at pages 6 and 7, and the description at page 5 of the 131 declaration describe the limitations of claims 1, 8, 13, and 24. For example, with reference to claim 8, the figure at page 6 illustrates memory hub and figure 7 illustrates a memory system having a plurality of memory modules that include respective memory hubs. The memory hub is illustrated as having a link interface for receiving memory requests for access at least one of the memory devices, a memory device interface (including a

cache, write buffer, and DRAM controller) for coupling to the memory devices (the memory devices shown in the figure at page 7), the memory device interface coupling memory requests to the memory devices for access to at least one of the memory devices (described in the description at page 5), a switch for selectively coupling the link interface and the memory device interface ("cross bar" shown in the figure of page 6), and a DMA engine coupled through the switch to the memory device interface, the DMA engine generating memory requests for access to at least one of the memory devices to perform DMA operations (illustrated in the figure at page 6 and described in the description at page 5). The limitations of claims 1, 13, and 24 are similarly described by the description at page 5 and the figures at pages 6 and 7. The sum of the description and figures in Attachment A exhibit "more than a vague idea of how to solve a problem," and illustrates a definite and permanent idea of the invention claimed by at least claims 1, 8, 13, and 24. Despite the Examiner's assertion that the 131 declaration is insufficient to establish a conception of the invention prior to the effective date of the Cheung reference, *see* the Office Action at page 10, conception of at least claims 1, 8, 13, and 24, as previously discussed, is established.

The Examiner further argues that the 131 declaration fails to establish due diligence to the filing date of the present application for constructive reduction to practice, citing MPEP section 2138.06. As set forth in that section, the period during which diligence is required must be accounted for by either affirmative acts or acceptable excuses. As further set out in MPEP section 2138.06, reasonable diligence does not require that "an inventor or his attorney . . . drop all other work and concentrate on the particular invention involved," citing *Emery v. Ronden*, 188 U.S.P.Q. 264 (Bd. Pat. Inter. 1974). *See* the MPEP section 2138.06. The affirmative acts taken by the inventor are stated in the 131 declaration, in particular, the inventor "reviewed drafts of the patent application . . . and provided [the attorney] with my comments and edits in the regular course of my work." *See* the 131 declaration, section 8. The inventor's review, comments, and edits exhibit affirmative acts to constructively reduce the invention to practice by finalizing the patent application for filing.

For the foregoing reasons, the 131 declaration establishes both conception prior to April 28, 2003, and due diligence to the filing of the present application, thereby removing the Cheung reference as prior art.

Even if the Examiner maintains that the 131 declaration is ineffective to overcome the Cheung reference, the combined teachings of the Leddige patent in view of the Cheung reference do not teach or suggest claims 1, 8, 13, and 24 as amended.

The Leddige patent describes a memory system having memory modules coupled to a memory controller through a series of memory repeater hubs. The memory repeater hubs are also coupled to the memory devices of the respective memory module. An example of a memory repeater hub 720 is illustrated in Figure 7 of the Leddige patent.

The Cheung reference describes a system on chip ("SoC") having an integrated DMA controller that is used for testing and verification of components of the SoC. Figure 1 of the Cheung reference illustrates a SoC 1 having a DMA controller 10 and Figure 2 illustrates the DMA controller 10 in greater detail. The DMA controller 10 includes a bus interface unit 110 that generates signals to form a required bus cycle for running and testing the module to be verified.

In contrast to the combined teachings of the Leddige and Cheung references, claims 1, 8, 13, and 24 recite a memory hub including an I/O register operable to store status information indicative of completion of a DMA operation and error status of the DMA operation, and the DMA engine is operable to program status information in the I/O register upon completion of the DMA operation. The Leddige patent does not describe a DMA controller, and the Cheung reference teaches a SoC including a DMA controller for testing and verification of modules coupled to the SoC. Neither the Leddige or Cheung reference teach an I/O register in a memory hub to which status information is written to by a DMA engine upon completion of DMA operations. As described in the present application and Exhibit A of the 131 declaration, an I/O register can be included in the memory hub for storing status information that can be used to identify whether the DMA operations have terminated normally with no errors, or abnormally due to errors. The status information can also be used to generate an interrupt to the host.

For the foregoing reasons, claims 1, 8, 13, and 24 are patentable over the Leddige patent in view of the Cheung reference. Claims 2, 5, and 6, which depend from claim 1, claim 9, which depends from claim 8, claims 14, 17, 18, 21, and 22, which depend from claim 13, and claims 26, 28, 29, 32, and 33, which depend from claim 24, are similarly patentable based on their dependency from respective allowable base claims. Therefore, the rejection of claims 1, 2,

5, 6, 8, 9, 13, 14, 17, 18, 21, 22, 24, 26, 28, 29, 32, and 33 under 35 U.S.C. 103(a) should be withdrawn.

As previously mentioned, the Examiner rejected claims 7, 12, 23, and 34 under 35 U.S.C. 103(a) as being unpatentable over the Leddige patent in view of the Cheung patent, and further in view of the Schmidt patent. Claims 4, 11, 20, and 31 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Leddige and Cheung patents, and further in view of the Jones reference. Claims 15, 16, 25, and 27, have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Leddige and Cheung patents, and further in view of the Frame reference.

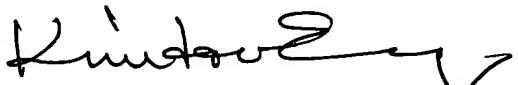
The Schmidt patent has been cited by the Examiner as teaching a next register in a DMA controller. *See* the Office Action at page 7. The Jones reference has been cited by the Examiner as teaching a crossbar switch. *See* the Office Action at page 8. The Frame reference has been cited by the Examiner as teaching a high-speed optical memory bus wherein the link interface of the memory hub comprises an optical memory bus interface circuit for translating optical signals and electrical signals. *See* the Office Action at page 9. Even if it is assumed that the Examiner's characterizations of the cited references are accurate, none of them make up for the deficiencies of the Leddige patent and the Cheung reference as previously discussed.

For the foregoing reasons, claims 4, 11, 12, 15, 16, 20, 23, 25, 27, 31, and 34, are patentable over the Leddige patent in view of the Cheung reference, in further view of the Schmidt patent, the Jones reference, or the Frame reference, alone or in combination. Therefore, the rejection of claims 4, 11, 12, 15, 16, 20, 23, 25, 27, 31, and 34, under 35 U.S.C. 103(a) should be withdrawn.

All of the claims pending in the present application are in condition for allowance. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

DORSEY & WHITNEY LLP



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